Remarks

This is in supplement to the Amendment filed on April 13, 2004 (entry of which is requested in the Request for Continued Examination filed herewith). Claims 1-6 remain pending. Reconsideration and allowance are respectfully requested in view of the following remarks.

Claims 1, 3, 4, and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kinoshita, U.S. Patent No. 5,869,852, in view of Young, U.S. Patent No. 6,229,861. This rejection is respectfully traversed, to the extent it is maintained.

Claim 1 recites arranging the power supply capacitor cell in a vicinity of the logic gate cell which is used to determine the capacitance value of the capacitor cell.

Therefore, claim 1 defines a relationship between the capacitance value of the capacitor cell and the drive load capacity value of the logic gate cell positioned in the vicinity of the capacitor cell. In other words, claim 1 recites not only determination of a capacitance value for the capacitor cell, but also recites determination of the capacitance value based on the logical gate cell and placement of the capacitor cell in the vicinity of the logic gate cell. In this configuration, the L-Element of wires in a power supply can be reduced, so that the power supply noise can be suppressed effectively. See page 7, line 36 - page 8, line 1 of the present application.

The rejection concedes that Kinoshita fails to disclose or suggest that a capacitance value of the power supply capacitor cell is determined using a drive load capacity value of the logic gate cell, as recited by claim 1.

Likewise, Young is silent with respect to determining the capacitance value of the power supply capacitor cell using the drive load capacity value of the logic gate cell which is located in the vicinity of the capacitance cell, as recited by claim 1.

For at least these reasons, neither Kinoshita nor Young, alone or in combination, disclose or suggest an LSI layout method including arranging the power supply capacitor cell in a vicinity of the logic gate cell which is used to determine the capacitance value of the capacitor cell, as recited by claim 1. Reconsideration and allowance of claim 1, as well as claims 3 and 4 that depend therefrom, are respectfully requested.

Claim 6 is similar to claim 1, except that claim 6 recites that the power supply capacitor cell is arranged adjacent to the logic gate cell. For similar reasons to those noted above with

respect to claim 1, neither Kinoshita nor Young render claim 6 obvious under section 103(a). Reconsideration and allowance are respectfully requested.

In view of the above supplemental remarks, favorable reconsideration of claims 1-6 in the form of a Notice of Allowance is requested. The Examiner is invited to contact the undersigned at (612) 371-5237 with any questions regarding this application.

Respectfully submitted,
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